vertical compute

Bits & Chips event - November 20th 2025

vertical compute

2011

Mark Andreessen
founder of Netscape,
renowned Venture Capitalist
Andreessen-Horowitz

Software is eating the world, in all sectors

In the future every company will become a software company

2017

— **“Software is eating the world, but AI is going to eat software“**

Jensen Huang in 2017

2025

Market Summary > NVIDIA Corp

139.98 USD

+139.94 (349,850.00%) ↑ all time

Feb 18, 13:41 EST • Disclaimer

1D 5D 1M 6M YTD 1Y 5Y Max

Open	141.27	Mkt cap	3.43T	52-wk high	153.13
High	143.44	P/E ratio	55.15	52-wk low	66.25
Low	138.98	Div yield	0.029%		

META - hyperion datacenter to reach the size of Manhattan

Bloomberg - Aug. 24th 2025

OpenAI's Stargate project to consume up to 40% of global DRAM output — inks deal with Samsung and SK hynix to the tune of up to 900,000 wafers per month

News By Anton Shilov published October 1, 2025

Working at scale.

Comments (9)

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Tom's Hardware - Oct. 1st 2025

How is Google Backing Fusion Future Data Centres?

By Ben Craske

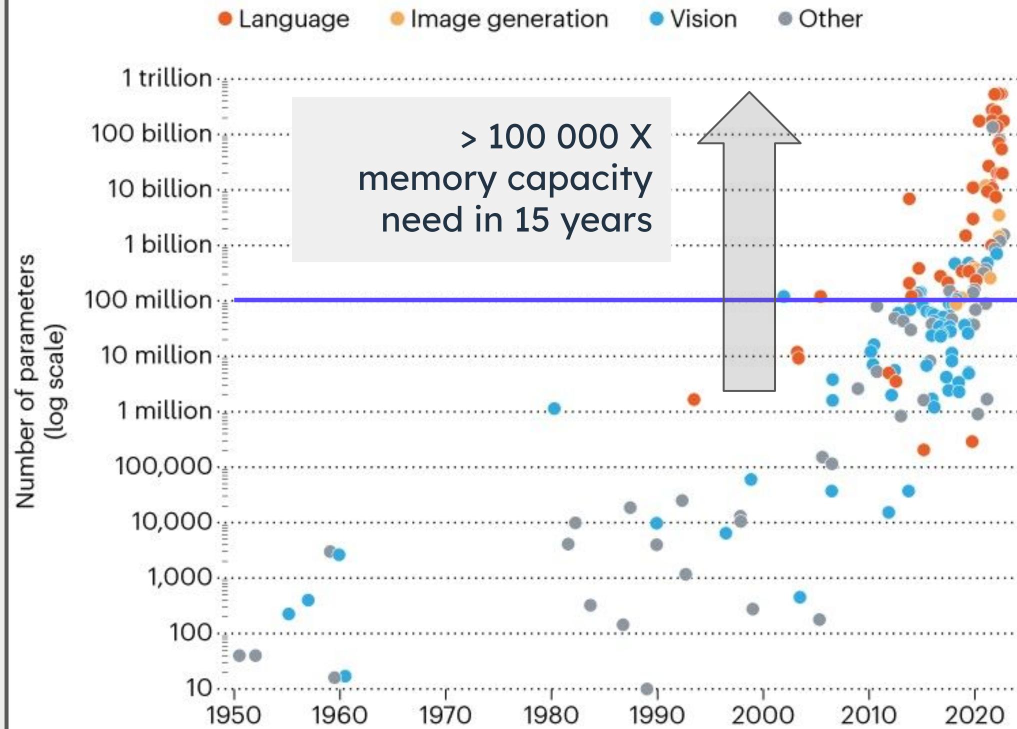
July 02, 2025 • 5 mins

Datacentre mag. - July 2nd 2025

GenAI infra becomes a societal, economic and geopolitical challenge

20 **Billion** parameters = 20 **GB** (int8)
min bandwidth for 100 Token/s = 100 * 20GB = 2TB/s

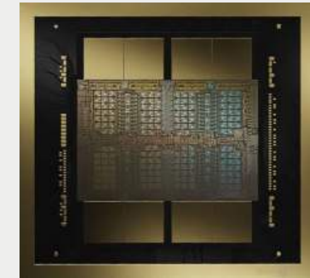
AI hardware - compute has a memory problem



[Nature 2023] doi: 10.1038/d41586-023-00777-9

Standalone memory + bus
Expensive datacenter multichip
Only solution for Gen AI

Nvidia B200 superchip



~ Integrated memory
Single chip options exists
Enable AI vision products

Tesla FSD chip

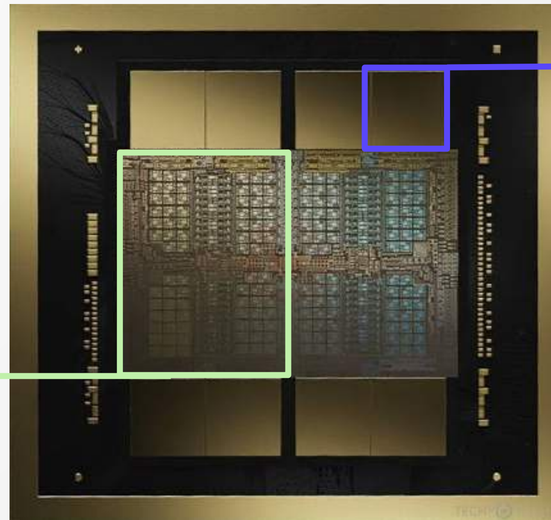
AI hardware - compute has a memory problem

GPU silicon chip

65% of the chip is memory

for the 1st gen

2 AI Compute dies



Nvidia B200 die shot

10,000$ HBMs

100$/GB

8 HBMs of 16 DRAM dies

because of that, AI is kept in the cloud, not in customers´hand

HBM: High Bandwidth Memory (Samsung, SK-Hynix, Micron)

An inconvenient thruth

DRAM cost scaling bottomed in 2012

DRAM becomes biggest BOM of datacenters

Introducing Disruptive Magnetic Vertical Integrated Memory

Vertical magnetic memory architecture at the core.

Re-uses 3D-NAND fabrication processes
→ high density, cost-effective and proven.

Re-uses magnetic domain walls physics
→ fast, low energy and unlimited endurance

Delivered as 3D chiplets
→ high bandwidth, modularity & scalability

Multiple bits stored vertically and read sequentially **at nanosecond speed**

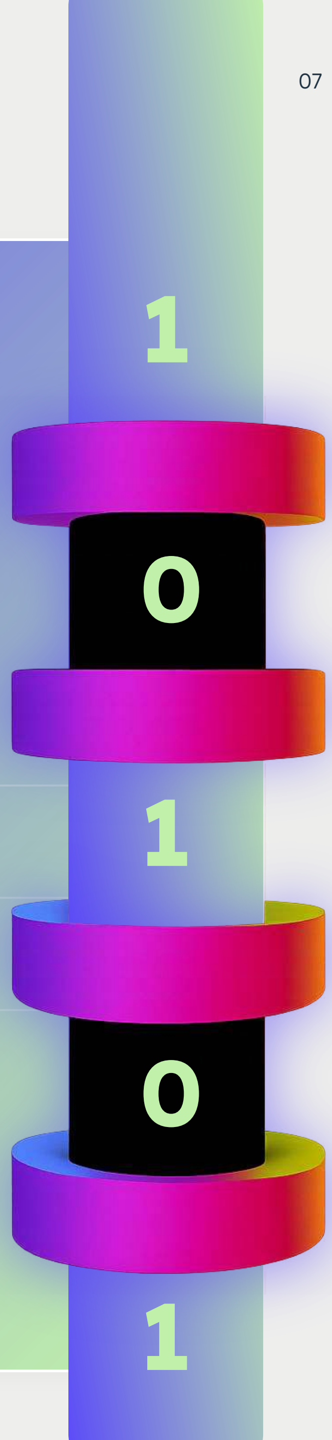
PERFORMANCE GAINS

Energy (no refresh, < pJ/bit)

Performance (> TB/s bandwidth)

Endurance (unlimited)

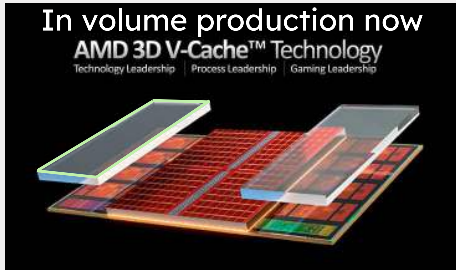
High temp support (>125 degC)



Vertical Compute’s product vision

Unlocking GenAI on device

3D-integrated (die to die) memory chiplet exists today…

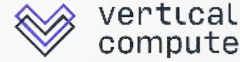


0,128 GB SRAM

But…

Not scaling anymore, with **generational density gain of |~1.1X**

First engineering samples in 2028



VIM 3D chiplet

5 GB VIM

N7 (integrated in BEOL)
Hybrid bonding

Targeted customers

AI compute (N5-N2,…)
Automotive (N28-N7, …)
Mobile & client (N16-N2, …)
Defense in-field context gen (…)

AMD Qualcomm

No path to single chip GenAI inference

Enables Single chip LLM inference
AI is unleashed from its datacenter chains

The promise - personalized GenAI on devices

No more continuous data transfert to DRAM (HBM or DDR)

No refresh - No standby power

ENERGY SAVING

INSTANT & HIGH PERFORMANCE

PRIVATE & SECURE

Always ready

Autonomous / Offline capable

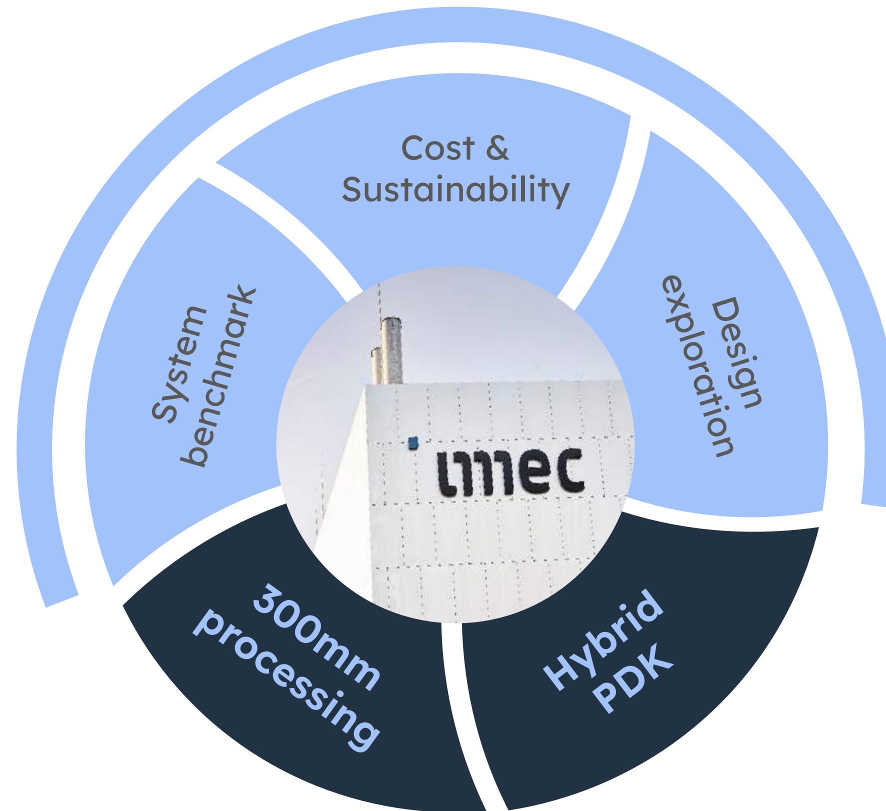
Continuous token generation (always on)

Customized models running on device data processing stay local

vertical compute

TRL elevation at Imec

Pre-seed activities



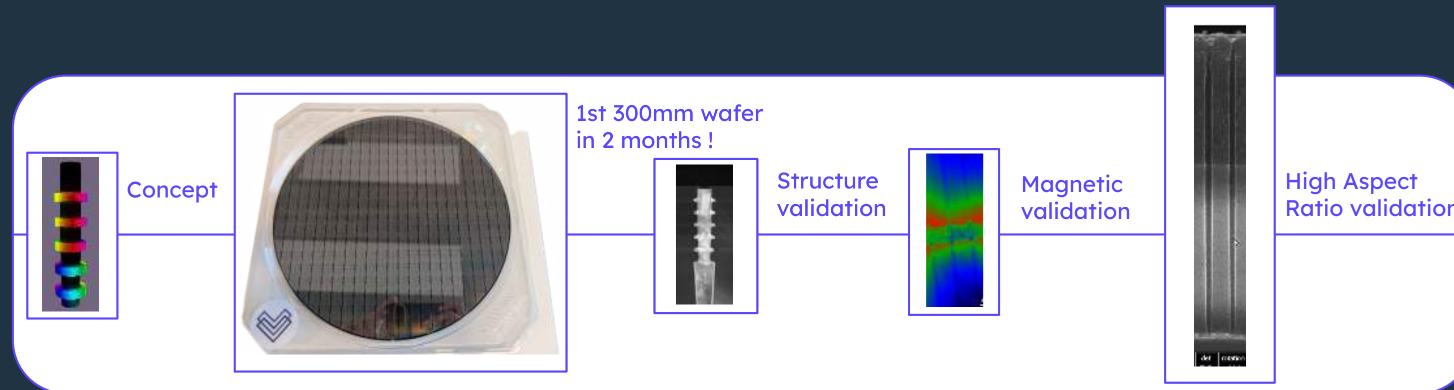
First tech unlocks

Operations launched (Imec spin-off)

Dec. 24

Pre-seed raised at inception

€20M



Technology Readiness Level 1
Basic Principles observed

Technology Readiness Level 5
Technology validated in lab in relevant environment (tools, foundry, process)

Wafers successfully produced & tested

121

Patent portfolio

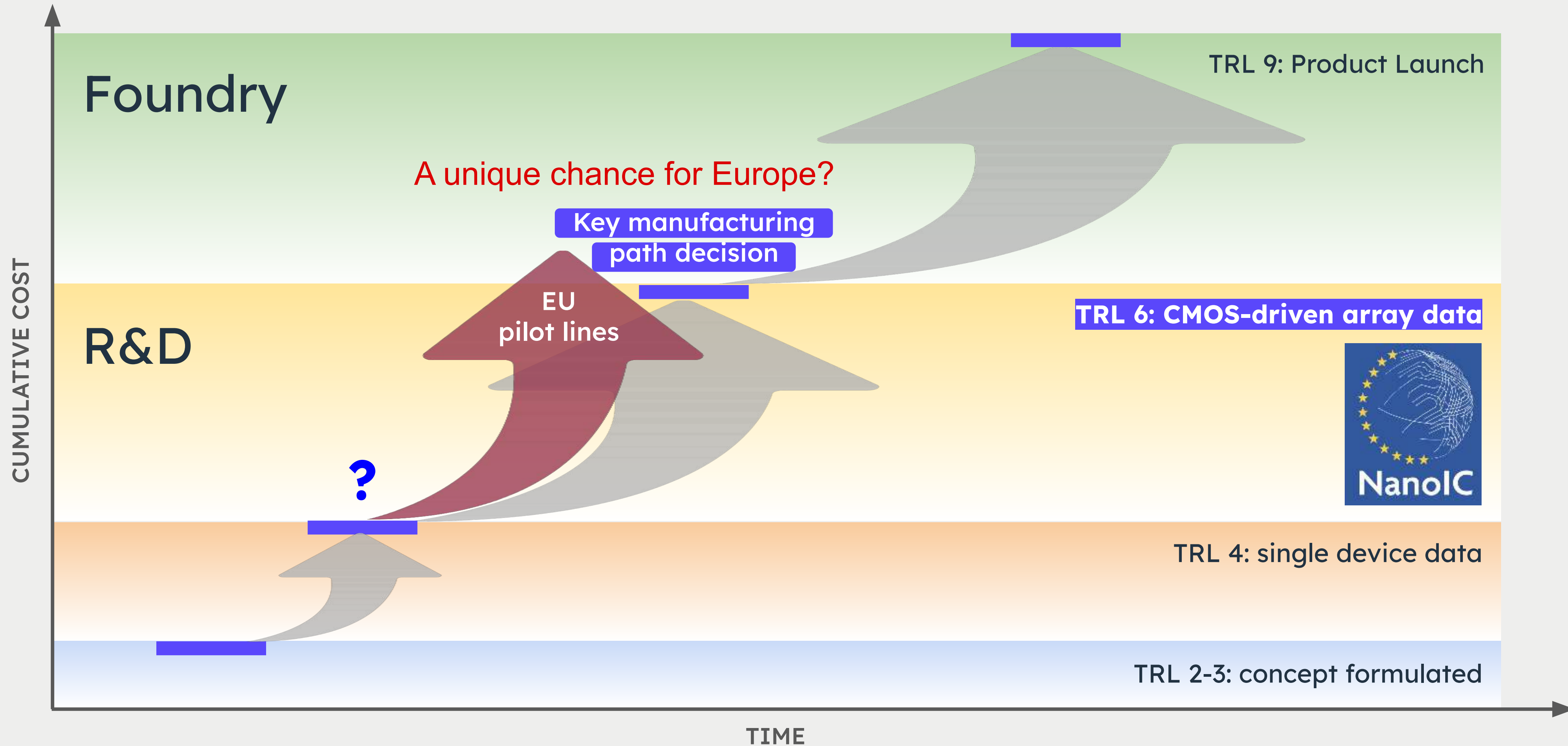
17

Test-chip design layout tape-out (Foundry+imec)

Q4-25

vertical compute

NanoIC pilot line to support us up to functional proto



vertical compute

Execution Roadmap

2025

Launch & build

€20m in pre seed funding

25 TEAM MEMBERS

Consolidation of IPs portfolio
(1 acquisition)

PoC of vertical memory elements
(write/push/read)

Test-chip design tape-out finalized

2026 - 2028

Partnership & acceleration

€30m in seed funding

+40 TEAM MEMBERS

MVP - First selling product
(50x SRAM density)

→ finished wafers compute & logic

→ full characterisation array

→ Eval kit

First partnership signed
with low volume back-end fab

Strengthening of the IPs portfolio

International expansion US/Asia

2028 - 2030

Deployment & scaling

+€100m in series A funding

+100 TEAM MEMBERS

3D chiplets in volume production
unlocking new applications

Co-design agreement signed with a large customer

Production ramp-up in a high volume
back-end fab (Asia/US/EU)

Tech evolution towards even
more density and performance

Revenue > **€300m**

IPO

The team

→ 25+ worldwide experts team
→ 30% women (incl. 100% Leuven Eng. team!)
→ Locations:
  - Leuven: HQ & Tech R&D
  - Grenoble: Chip design and systems

→ 20 MEur Seed funding

Head of technology

San José, CA

We are ecosystem partners and enablers

vertical
compute

sebastien@verticalcompute.com

Strictly confidential